IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/618,828	Examiner:	Truong, Camquy
Filed:	July 14, 2003	Group/Art Unit:	2195
Inventors:		Atty. Dkt. No:	5681-15100/P7636
Ajay Kumar, et al.			
Title:	Transaction Manager Freezing		

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

Applicants respectfully request review of the rejection in the above-identified application. Claims 1-36 are pending in the application. Please note that for brevity, only primary arguments are presented. Additional arguments may be presented if and when the case proceeds to Appeal. The Examiner rejected the independent claims as being unpatentable over Hagersten et al. (U.S. Patent 5,983,326) (hereinafter "Hagersten") in view of Fowler (U.S. Patent 4,502,116). The following **clear errors** in the Examiner's rejection are noted.

Independent Claim 1:

1. The cited art fails to teach or suggest *program instructions executable to implement a transaction manager that manages a plurality of transactions, wherein each transaction comprises a plurality of operations to one or more data sources.*

Claim 1 recites a transaction manager implemented in software, i.e., executable program instructions. In contrast, the functionality in Hagersten relied upon by the Examiner to teach the transaction manager of claim 1 is part of the hardware circuitry of system interface 24. The Examiner refers to the fact that Hagersten describes memory that includes code for use by its processors. However, the code in Hagersten's memory is not described as executable by the one or more processors to implement a transaction manager. In fact, the functionality in Hagersten relied upon by the Examiner to teach the transaction manager of claim 1 is part of system interface 24, **which is a hardware interface and is separate from memory 22 and processors 16, and not at all implemented by any code stored in memory 22**. See Hagersten, col. 7, lines 44-53 cited by the Examiner. Hagersten's home agent and system interface are not described as being implemented by program instructions stored in memory 22 or any other memory. In the instant Advisory Action, the Examiner states, "Hagersten teaches a home agent for use within a node of a multiprocessing computer system comprising a plurality of storage elements (memory) configured to receive transaction requests (program instructions) from the other nodes…"

Applicants assert there is no support in Hagersten for a transaction request that includes program instructions, as asserted by the Examiner in the Advisory Action. In fact, it would not make sense or even be possible for the transaction request to include program instructions that somehow implement the transaction manager, as the Examiner seems to be implying in the Advisory Action. The home agent referenced by the Examiner is part of hardware system interface 24 which is the **hardware** interface between the hardware signals of SMP bus 20 and the hardware signals of network 14. The home agent in Hagersten could not possibly execute in software because it must operate on hardware signals before they ever reach a processor 16. In general, Hagersten has essentially no relevance to a transaction manager as recited in claim 1. Hagersten uses the term "transaction" to refer to hardware bus communications, not transactions managed in software. Also, the teachings in Fowler relied upon by the Examiner refer to a hardware toggle switch. Neither reference has anything at all to do with a transaction manager implemented in software.

2. The cited art fails to teach or suggest that *each transaction comprises a plurality of operations to one or more data sources that are required to be committed to the one or more data sources atomically for each respective transaction.*

The Examiner refers to col. 8, lines 20-34, of Hagersten. However, Hagersten does not teach that each individual transaction comprises a plurality of operations. To the contrary, the cited portion of Hagersten states that a transaction includes at most a single memory operation. Also, the cited portion of Hagersten says nothing of each individual transaction comprising a plurality of operations that are required to be committed to the one or more data sources atomically for each respective transaction. In the instant Advisory Action, the Examiner states, "Hagersten teaches a given processor performs an atomic operation to obtain access to a critical memory region." (emphasis added). The Examiner refers to column 1, lines 14-25. This passage refers to a spin-lock operation used to obtain access to a memory region, which has nothing to do with committing a plurality of operations to one or more data sources. Also, the Examiner appears to agree that a transaction in Hagersten corresponds to a single operation, not a plurality of operations to all be atomically committed.

3. The cited art fails to teach or suggest that *the transaction manager is configured to pause the plurality of transactions managed by the transaction manager in response to a pause request to pause the transaction manager, wherein while paused, the transaction manager does not allow any of the plurality of transactions managed by the transaction manager to complete.*

The Examiner cites Hagersten, column 5, lines 55-64; column 7, lines 44-53, and column 17, lines 7-9. These passages teach one or more queues configured to receive transaction requests from processing nodes. The passages also teach a home agent control unit configured to receive and service transaction

requests and a transaction blocking unit coupled to the queues and the home agent. For example, column 5, lines 60 through column 6, line 4 states:

> The transaction blocking unit is configured to block selected transactions if another transaction request to a common coherency unit is currently being serviced by the home agent control unit. The transaction blocking unit is further configured to allow servicing of a given transaction request to a particular coherency unit if a second transaction request to the particular coherency unit is currently being serviced by the home agent control unit and if the second transaction request does not cause ownership of the particular coherency unit and if the second transaction request and the given transaction request are the same transaction type.

The transaction blocking unit of Hagersten clearly does not block transactions in response to a pause request as required by Applicants' claim 1. Instead, the transaction blocking unit blocks a second transaction if a first transaction request (to a common coherency unit) is currently being serviced by the home agent. The transaction blocking unit is not responding to a request to pause, but rather is responding to the detection of a second transaction request arriving when the home agent is servicing a first transaction request. Hagersten, whether or not combined with Fowler, does not teach pausing **all** transactions managed by the transaction manager in response to a pause request as required by Applicants' claim 1. To the contrary, Hagersten explicitly allows the current transaction to complete while blocking one or more other transactions.

4. The cited art fails to teach or suggest that the transaction manager is configured to resume the plurality of transactions managed by the transaction manager in response to a resume request.

The Examiner cites column 17, lines 9-12, which states, "...subsequent requests involving the coherency unit are not performed until the coherency activity corresponding to the coherency request is completed." Hagersten teaches activity is resumed when the coherency unit completes the current task. Clearly there is no resume request taught by Hagersten. The Examiner also cites Fowler, column 5, lines 40-53 and column 8, lines 52-56. Column 5, lines 40-43 state, "The control section 80 of the Subsystem Synchronization Interface circuit provides users with toggle switches to configure the pause/resume synchronization of the multiprocessor system." **A manual toggle switch that causes processors to pause has absolutely nothing to do with the teachings of Hagersten or with the limitations of claim 1.** Neither Hagersten or Fowler teach pausing transactions managed by the transaction manager in response to a pause request to pause the transaction manager. Neither reference has anything at all to do with a transaction manager in software that receives a pause request to pause all managed transactions, and that resumes managed transactions in response to a resume request.

5. The Examiner's proposed combination makes no sense and would be inoperable.

The transactions in Hagersten are paused and resumed in hardware in response to detection of very specific hardware events. For example, Hagersten's transaction blocking unit blocks a second transaction if a first transaction request (to a common coherency unit) is currently being serviced by the home agent.

It would make absolutely no sense whatsoever to modify Hagersten to instead pause a transaction in response to a signal from a manual toggle switch as taught by Fowler. **In fact, given that Hagersten's transactions are high speed hardware bus communications, it would be impossible to pause such a transaction with a manual toggle switch, as taught by Fowler.** Furthermore, the pause request in Fowler is to pause the entire processor, not a single transaction. The Examiner's proposed modification of Hagersten would destroy the intended operation of Hagersten's system. "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). In the instant Advisory Action the Examiner states, "**the motivation is a soft profile of the thread will not damaging the ligament while still provides resistant of pullout (see 'Hubbard' col. 4, lines 7-12).**" Applicants assert the Examiner's comment is nonsensical and not relevant. Furthermore, Hubbard is not a reference of record.

Independent Claim 14:

1. **The cited art fails to teach or suggest *program instructions executable by the one or more processors to implement one or more application servers, wherein each one or more application servers is configured to run one or more applications … and provide one or more transaction managers.***

As described above in regard to claim 1, the portions of the cited art cited by the Examiner are all hardware circuits, not program instructions. Furthermore, it would not be possible for the home agent in Hagersten to be implemented in software because it is part of the hardware interface between the SMP bus and the network. Neither Hagersten not Fowler has anything at all to do with transaction managers implemented in software. Hagersten uses the term "transaction" to refer to hardware bus communications, not transactions managed in software.

2. **The cited art fails to teach or suggest that *each of the one or more transactions comprises a plurality of operations to one or more data sources that are required to be committed to the one or more data sources atomically for the transaction.***

To the contrary, the cited portion of Hagersten states that a transaction includes at most a single memory operation. In the Advisory Action, the Examiner appears to agree that a transaction in Hagersten corresponds to a single operation, not a plurality of operations to all be atomically committed.

3. **The cited art fails to teach or suggest that *one of the transaction managers is configured to pause a corresponding one or more transactions in response to a pause request and to resume the corresponding one or more transactions in response to a resume request, wherein while paused, the transaction manager does not allow the corresponding one or more transactions to complete.***

As discussed above in regard to claim 1, neither Hagersten not Fowler, alone or in combination, teaches or suggest a pause request and a resume request as recited for Applicants' claimed invention.

4. The Examiner's proposed combination makes no sense and would be inoperable.

As discussed above in regard to claim 1, the Examiner is attempting to combine the references in a manner that makes no sense and is counter to their intended operation. The proposed combination is clearly improper.

Independent Claims 15 and 26:

1. The cited art fails to teach or suggest *each transaction managed by the transaction manager comprises a plurality of operations to one or more data sources that are required to be committed to the one or more data sources atomically for each respective transaction.*

To the contrary, the cited portion of Hagersten states that a transaction includes at most a single memory operation. In the Advisory Action, the Examiner appears to agree that a transaction in Hagersten corresponds to a single operation, not a plurality of operations to all be atomically committed.

2. The cited art fails to teach or suggest *generating a request to pause a transaction manager; pausing the transaction manager in response to said request to pause the transaction manager; generating a request to resume the transaction manager; and resuming the transaction manager in response to said request to resume the transaction manage.*

As discussed above in regard to claim 1, neither Hagersten not Fowler, alone or in combination, teaches or suggest a pause request and a resume request as recited for Applicants' claimed invention. The home agent in Hagersten blocks transactions based on detecting the state of an existing transaction, **not in response to any request**.

3. The Examiner's proposed combination makes no sense and would be inoperable.

As discussed above in regard to claim 1, the Examiner is attempting to combine the references in a manner that makes no sense and is counter to their intended operation. The proposed combination is clearly improper.

The Examiner also provisionally rejected claims 1-36 under the judiciary created doctrine of double patenting over claims 1-56 of copending Application No. 10/618,810. If this rejection becomes non-provisional, Applicants will either submit a terminal disclaimer or present arguments traversing the rejection.

Respectfully submitted,
/Robert C. Kowert/
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